REMARKS

A. Introduction

Claims 1-8 were pending and under consideration in the application.

In the Office Action of December 24, 2008 claims 1, 2, and 8 were rejected under 35 U.S.C. §102(b), as being anticipated by Harding, et al., US Pub 2003/0005277 (hereinafter, "*Harding*").

Claim 3 was rejected under 35 U.S.C. §103(a), as being unpatentable over *Harding* in view of Hashimoto, JP57-071508 (hereinafter, "*Hashimoto*").

Claims 4 and 5 were rejected under 35 U.S.C. §103(a), as being unpatentable over *Harding* in view of Dawson, et al., (U.S. 6,311,213) (hereinafter, "*Dawson*").

Claim 6 was rejected under 35 U.S.C. §103(a), as being unpatentable over *Harding* in view of *Dawson*, and further in view of Kim, U.S. 6,587,915, (hereinafter, "*Kim*").

Claim 7 was rejected under 35 U.S.C. §103(a), as being unpatentable over *Harding* in view of *Hashimoto*, and further in view of Aasheim, et al., U.S. 7,178,061, (hereinafter, "*Aasheim*").

In response, claims 1 and 8 are being amended for clarity. Support for the amendment may be found, at least at paragraph 0054 of the application as published as US 2008/0046637. Accordingly, no new matter is being added.

B. Rejections under 35 U.S.C. 102(b)

Claims 1, 2, and 8 were rejected under 35 U.S.C. §102(b), as being anticipated by *Harding*.

Harding discloses a dual-Basic Input/Output System (BIOS) system, wherein a primary BIOS image and a backup BIOS image are stored in a programmable read-only memory. In the event the primary BIOS image is faulty, the back-up BIOS image is automatically enabled. *Harding*, ¶'s 0010-0012. Thus, a fault in the primary BIOS image may be mitigated by use of the backup BIOS image, provided that the entirety of the backup BIOS image is faultless.

Harding fails to teach or suggest a memory having a plurality of data blocks for storing boot program instructions having a plurality of pages of data, where each said page is stored in parallel in at least two respective data blocks, and, for each page of data, a read control circuit (a) determines whether the first respective data block is faulty or not according to first data read out from the first respective data block, (b) outputs the first data to a CPU when the first data block is determined as not faulty, (c) reads, when the first respective data block is determined as faulty, second data from the second respective data block and outputs said second data to the CPU when said second respective data block is determined as not faulty.

A finding that a claim is anticipated requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F. 2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Because *Harding* fails to disclose at least the features of the claims discussed above, independent claims 1 and 8, and claim 2, which depends from claim 1, are patentable over *Harding*.

C. Rejections under 35 U.S.C. 103(a)

1. Claim 3 was rejected under 35 U.S.C. §103(a) as being unpatentable over *Harding* in view of *Hashimoto*.

Hashimoto is cited for disclosing a read control circuit correcting data and supplying it to the CPU when it determines that the data is correctable according to an

error correction code. Whether or not this is true, such disclosure fails to cure the deficiencies noted above. As a result, claim 3 is patentable over the combination of *Harding* and *Hashimoto*.

2. Claims 4 and 5 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Harding* in view *Dawson*.

Dawson is cited for disclosing determining that a data block is faulty or not faulty according to a block state information. Whether or not this is true, such disclosure fails to cure the deficiencies noted above. As a result, claims 4 and 5 are patentable over the combination of *Harding* and *Hashimoto*.

3. Claim 6 was rejected under 35 U.S.C. §103(a) as being unpatentable over *Harding* in view of *Dawson*, and further in view *Kim*.

Kim is cited for disclosing storing of block state information in a leading page of a data block. Whether or not this is true, such disclosure fails to cure the deficiencies noted above. As a result, claim 6 is patentable over the combination of *Harding*, *Dawson* and *Kim*.

4. Claim 7 was rejected under 35 U.S.C. §103(a) as being unpatentable over *Harding* in view of *Hashimoto*, and further in view of *Aasheim*.

Assheim is cited for disclosing a NAND type flash memory. Whether or not this is true, such disclosure fails to cure the deficiencies noted above. As a result, claim 7 is patentable over the combination of *Harding* and *Hashimoto*.

D. Conclusion

In view of the foregoing, it is submitted that claims 1-8 are allowable and that the application is in condition for allowance. Early notice to that effect is respectfully requested.

If the Examiner believes that, for any reason, direct contact with Applicants' attorney would help advance the prosecution of this case to finality, the Examiner is invited to telephone the undersigned at the number given below, for purposes of arranging for a telephonic interview. Any communication initiated by this paragraph should be deemed an Applicant-Initiated Interview.

If any further fees are required in connection with the filing of this amendment, please charge the same to our Deposit Account No. 19-3140.

	Respectfully submitted, SONNENSCHEIN NATH & ROSENTHAL LLP
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